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10/586,846	07/20/2006	Ingrid Verbauwhede	UCLARF.004NP	3453

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EXAMINER
TABLER, MATTHEW C

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
08/12/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/586,846	VERBAUWHEDE ET AL.	
	Examiner	Art Unit	
	MATTHEW C. TABLER	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-12 and 23-26* is/are pending in the application.

4a) Of the above claim(s) *1,2 and 13-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *3-12 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's remarks filed on May 7th, 2009. Currently, claims 3-12 and 23-26 are pending.

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-4, 7-8 and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Davies et al. (US Patent 6,329,846) patented on December 11th, 2001.

Regarding claim 3, Davies et al. show a wave dynamic differential logic (Figure 5), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide

one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), said differential logic cell configured to propagate a pre-discharge wave (cross-coupled outputs provide pre-discharge for the output signals).

Regarding claim 4, Davies et al. show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), and a pre-discharged logic cell configured to generate a pre-discharge wave to pre-discharge said differential logic cell (cross-coupled outputs provide pre-discharge for the output signals).

Regarding claim 7, Davies et al. show a first logic tree configured to receive inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B) and to produce one or more first outputs (outputs AB & ~AB), and a dual of said first logic tree configured to receive said inverted inputs and said corresponding non-inverted inputs (inputs A, ~A, B & ~B) and produce one or more inverted first outputs (outputs AB & ~AB).

Regarding claim 8, Davies et al. show a wave dynamic differential logic wherein a differential logic cell transmits a precharge value generated by a precharge generator (cross-coupled outputs provide pre-discharge for the output signals).

Regarding claim 23, Davies et al. show the wave dynamic differential logic comprising positive logic (see Figure 5).

Regarding claim 24, it has been rejected on the same grounds as claim 23.

Regarding claim 25, it has been rejected on the same grounds as claim 23.

Regarding claim 26, it has been rejected on the same grounds as claim 23.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davies et al. in view of Forbes (US Patent 6,437,604) patented on August 20th, 2002 and *design choice* case law.

Regarding claim 5, Davies et al. show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs AB & ~AB).

Davies fails to show circuitry for pre-charging the differential logic cell.

Forbes teaches circuitry for pre-charging the differential logic cell. More specifically, Forbes teaches a circuit to generate a pre-charge wave to pre-charge said differential logic cell (Figure 6, components 62 and 64 provide pre-charging in the same manner that Davies et al. discloses pre-discharging).

It would have been obvious to one skilled in the art, at time invention was made, to use pre-discharging circuitry, with the motivation that the outputs are more stable and

reduce power consumption as known by those of ordinary skill in the art as having a reasonable expectation of success.

Davies in combination with Forbes disclose the claimed invention expect for a master-slave differential dynamic logic register for generating a pre-charge signal.

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-charge circuitry shown by Forbes.

Regarding claim 6, Davies in combination with Forbes show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), and a master-slave differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell (cross-coupled outputs provide pre-discharge for the output signals).

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-discharge circuitry shown by Davies et al.

Regarding claim 9, Davies in combination with Forbes show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs

(outputs AB & ~AB) and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), and a master-slave differential dynamic logic register configured to transmit on a pre-charge wave to pre-charge said differential logic cell (Forbes – pre-charge circuitry 62 and 64 in Figure 5).

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-charge circuitry shown by Forbes.

Regarding claim 10, Davies in combination with Forbes show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs (outputs AB & ~AB) and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), and a differential dynamic logic register configured to generate a pre-charge wave to pre-charge said differential logic cell (Forbes – pre-charge circuitry 62 and 64 in Figure 5).

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-charge circuitry shown by Forbes.

Regarding claim 11, Davies in combination with Forbes show a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs A, ~A, B & ~B), said differential logic cell configured to provide one or more inverted logic outputs

(outputs AB & ~AB) and corresponding one or more non-inverted logic outputs (outputs AB & ~AB), and a master-slave differential dynamic logic register configured to transmit on a pre-discharge wave to pre-discharge said differential logic cell (cross-coupled outputs provide pre-discharge for the output signals).

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-discharge circuitry shown by Davies et al.

Regarding claim 12, Davies in combination with Forbes show a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell (cross-coupled outputs provide pre-discharge for the output signals).

It would have been an obvious matter of design choice to use a master-slave logic register and since applicant has not disclosed that a register solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with the pre-discharge circuitry shown by Davies et al.

Response to Arguments

Applicant's arguments filed 5/7/2009 have been fully considered but they are not persuasive.

With regard to claims 3-4, 7-8 and 23-26, the applicant argues that Davies et al. fail and states "the gate (of 410 and 411) does not propagate the precharge signal, rather the precharge signal must be provided by the clock."

The examiner wishes to clarify the record. The Davies et al. reference is intended to show pre-discharge functionality. More specifically, Davies et al. show the circuit outputs (AB and ~AB) coupled to discharge transistors 410 and 411 respectively. These transistors pull the output nodes down so that it may discharge more rapidly. No clock signal is required for pre-discharge. The applicant also notes that "the pre-discharge wave is propagated from the logic outputs of one stage to the logic inputs of the next stage." The examiner agrees with this assessment because the outputs of the circuit are also used for discharging the output nodes.

With regard to claims 5-6 and 9-12, the applicant argues that Davies et al. fail and states "the gate (of 410 and 411) does not propagate the precharge signal as a precharge wave, rather the precharge signal must be provided by the clock."

As mentioned before, the examiner disagrees because Davies et al. fails to show use of the output signals to 'precharge' the output signals. Only 'pre-discharge' is explicitly disclosed. Forbes however teaches a very similar circuit in Figure 6 that discloses two differential output nodes having a similar cross-coupled connection for 'precharge' of the output signals. No clock signal is required for precharge.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819
August 10, 2009

/Vibol Tan/
Primary Examiner, Art Unit 2819